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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/801,821

06/22/2004

Fumio Koyama

111587.01

2538

25944

7590

08/18/2005

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EXAMINER

MULPURI, SAVITRI

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 08/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	<b>Application No.</b>		<b>Applicant(s)</b>	
	10/801,821		KOYAMA ET AL.	
	<b>Examiner</b>		<b>Art Unit</b>	
	Savitri Mulpuri		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 09 May 2005.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-10 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-10 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)               | Paper No(s)/Mail Date. _____  |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date <u>2/18/2005</u>   | 6) <input type="checkbox"/> Other: _____                                    |

### **DETAILED ACTION**

This action is in response to the applicant's communications filed on IDS filed on 2/18/2005 and amendment to claims filed on 5/9/2005.

It is noted that Applicant did not argue over applied art, and Applicant amended the claim 1, line 10 added "plurality" before "specific oscillation modes" and added claims 6-10 as new claims, which are exactly same as original claims 1-5.

#### ***Claim Objections***

Claims 6, 7, 10 objected to because of the following informalities: Etching preventing not proper. Appropriate correction is required. It is suggested to replace with "etch preventing"

#### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 3-4, 6, 8, 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Kopan (EP 1,028,505).

Kopan teaches a method of making surface emitting semiconductor by the following process steps: Forming lower reflection layer "5", active layer (inherently quantum well layer) "1", upper reflection layer "3" in sequence forms laminate structure on a main surface of the semiconductor substrate "9" as recited in claims 1, 3 and 4;

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forming a post portion in the shape of the pillar with at least the upper reflection layer partially remaining; forming a grid layer "4" on a surface layer "2", wherein grid layer has plurality of openings "6", which are same as boundary regions as recited in instant claims, for suppressing light emission of oscillation modes except for specific oscillation modes; and substantially forming light emitting spots corresponding to the specific oscillation modes by processing a part of the region of the surface of the upper reflection layer which is exposed to the surface of the post portion (see fig. 1 and related description).

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Martinson et al (IEEE Photonics Technology Letters 1999) in combination with Shieh et al (US 5,293,392).

Martinson et al teaches a method of making surface emitting semiconductor by the following process steps: Forming on a main surface the semiconductor substrate successively forming lower reflection layer, active layer, and top reflection layer, wherein the successive layers in sequence forms laminate structure as recited in claims

8, 9; forming a metal contact layer ; forming a post portion in the shape of the pillar with at least the upper reflection layer partially remaining ; forming a boundary region for suppressing the light emission of oscillation modes except for specific oscillation mode; and substantially forming light emitting spot corresponding to the specific oscillation mode by processing a part of the region of the surface of the upper reflection layer, which is exposed to the surface of the post portion (see publication from IDS, for fig 1, 3a-3b and page 1041, right column).

Martinsson et al does not each (1) surface layer on the top of the upper reflection layer (2) etch preventing layer on the lower side of the surface layer.

Sheih et al teaches, prior to forming metal contact layer, forming transparent doped semiconductor contact layer "22" on the upper mirror layer "18"; and then followed by metal contact. Shieh et al also teaches etch stop layer "20" on the lower side of the contact layer. It would have been obvious to one of ordinary skill in the art to form semiconductor layer prior to the formation of metal contact in the invention of Martinsson et al because such contact layer would act as a surface layer as recited in instant invention and would give the advantage of the improved ohmic contact in the invention of Martinsson et al because such contact layer acts as a surface layer as recited in instant claims and give the advantage of improved ohmic contact for VCSEL and at the same time act as a light emission region because such layer would be transparent layer for light emission. It also would have been obvious to one of ordinary skill in the art to form etch stop layer underneath the surface layer "2" in the invention of the Kopan because etch stop would control the depth of the mesa emitting area, thereby

obtaining mesa structure with intended depth confining current flow and lasing to the mesa (see abstract).

Claims 2, 5, 7, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kopan (EP 1, 028,505) in combination with Shieh et al (US 5,293,392).

Kopan teaches a method of making surface emitting semiconductor by the following process steps: Forming lower reflection layer "5", active layer "1", upper reflection layer "3" in sequence forms laminate structure on a main surface of the semiconductor substrate "9" as recited in claims 1,3 and 4; forming a post portion in the shape of the pillar with at least the upper reflection layer partially remaining; forming a grid layer "4" on a surface layer "2", wherein grid layer has plurality of openings "6", which are same as boundary regions as recited in instant claims, for suppressing light emission of oscillation modes except for plurality specific oscillation modes; and substantially forming light emitting spots corresponding to the specific oscillation modes by processing a part of the region of the surface of the upper reflection layer which is exposed to the surface of the post portion (see fig. 1 and related description).

Kopan does not teach etch preventing layer on the lower side of the surface layer.

Sheih et al teaches, prior to forming metal contact layer, forming transparent doped semiconductor contact layer "22" on the upper mirror layer "18"; and then followed by metal contact. Shieh et al also teaches etch stop layer "20" on the lower side of the contact layer. It also would have been obvious to one of ordinary skill in the

art to form etch stop layer underneath the surface layer"2" in the invention of the Kopan because etch sop would control the depth of the mesa emitting area, thereby obtaining mesa structure with intended depth confining current flow and lasing to the mesa (see abstract).

### ***Conclusion***

Applicant's arguments with respect to claims 1-10 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Savitri Mulpuri whose telephone number is 571-272-1677. The examiner can normally be reached on Mon-Fri from 8 a.m to 4.30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt, can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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A handwritten signature in black ink, appearing to read 'Savitri Mulpuri', with a stylized, flowing script.

Savitri Mulpuri  
Primary Examiner  
Art Unit 2812